[025] What is claimed is:

[026] 1. A method for operating a integrated device within an operating range comprising:

enabling a reduced power operating mode in response to a predetermined condition for the integrated device;

changing the integrated device's voltage from a first voltage to a second voltage upon activation of the reduced power operating mode; and

operating the integrated device at a frequency within the operating range based at least in part on a desired amount of power reduction.

[027] 2. The method of claim 1 wherein the first voltage is a nominal operating voltage and the second voltage is a reduced voltage that is defined during manufacturing of the integrated device.

[028] 3. The method of claim 1 wherein the predetermined condition is either one of a thermal issue or a power issue.

[029] 4. The method of claim 2 wherein the second voltage is stored into a plurality of fuses.

[030] 5. The method of claim 1 wherein the bus ratio utilized in the power reduction

operating mode is less than a maximum bus ratio for the integrated device and is calculated based on subtracting an offset from the maximum bus ratio, the offset is based at least in part on the supported bus frequency of the integrated device.

[031] 6. The method of claim 1 wherein the integrated device is a processor.

[032] 7. A method for selecting a bus ratio for a reduced power operating mode of an integrated device comprising:

receiving a bus frequency that is supported by the integrated device;

selecting one of a plurality of offset values based at least in part on the bus frequency;

defining the bus ratio for the reduced power operating mode based at least in part on a startup bus ratio and the offset; and

operating the integrated device at the defined bus ratio in response to a need to reduce power consumption unless the maximum bus ratio is less than a predetermined bus ratio.

[033] 8. The method of claim 7 wherein the predetermined bus ratio is a minimum bus ratio that is supported by the integrated device.

[034] 9. The method of claim 7 wherein the plurality of offset values is calculated based on a projected power estimate and are coded in the logic of the integrated device.

[035] 10. The method of claim 7 wherein the bus ratio is defined by subtracting the selected offset value from the startup bus ratio.

[036] 11. The method of claim 7 further comprising choosing an alternate reduced power operating mode if the maximum bus ratio is less than a predetermined bus ratio.

[037] 12. The method of claim 10 wherein the integrated device is a processor.

[038] 13. A method for defining a reduced power operating mode for a integrated device comprising:

testing a integrated device to determine an operating voltage for the reduced power operating mode;

storing the reduced power operating voltage within a plurality of fuses;

receiving a bus frequency that is supported by the integrated device;

selecting one of a plurality of offset values based at least in part on the bus frequency;

defining a bus ratio for the reduced power operating mode based at least in part on a startup bus ratio and the offset; and

operating the integrated device at the bus ratio in response to a desire to reduce power consumption unless the maximum bus ratio is less than a predetermined bus ratio.

[039] 14. The method of claim 13 wherein the predetermined bus ratio is a minimum bus ratio that is supported by the integrated device.

[040] 15. The method of claim 13 wherein the plurality of offset values is calculated based on a projected power estimate and are coded in the logic of the integrated device.

[041] 16. The method of claim 13 wherein the bus ratio is defined by subtracting the selected offset value from the startup bus ratio.

[042] 17. The method of claim 13 further comprising choosing a different reduced power operating mode if the desired reduced power operating mode bus ratio is less than the predetermined minimum bus ratio.

[043] 18. The method of claim 17 wherein the integrated device is a processor.

[044] 19. A circuit to determine a bus ratio for a reduced power operating mode of a integrated device comprising:

a multiplexer to receive a plurality of offset values and a bus frequency that is supported by the integrated device and to forward one of the offset values based at least in part on the bus frequency;

a logic to define the reduced power bus ratio as a startup bus ratio minus the selected offset value; and

to operate the integrated device at the bus ratio unless the bus ratio is less than a predetermined bus ratio.

[045] 20. The circuit of claim 19 wherein the predetermined bus ratio is a minimum bus ratio that is supported by the integrated device.

[046] 21. The circuit of claim 19 wherein the plurality of offset values is calculated

based on a projected power estimate and are coded into RTL.

[047] 22. The circuit of claim 19 further comprises to utilize a different reduced power operating mode if the maximum bus ratio is less than the predetermined bus ratio.

[048] 23. The circuit of claim 21 wherein the integrated device is a processor